

# SSI2164

## FATKEYS™ QUAD VOLTAGE CONTROLLED AMPLIFIER

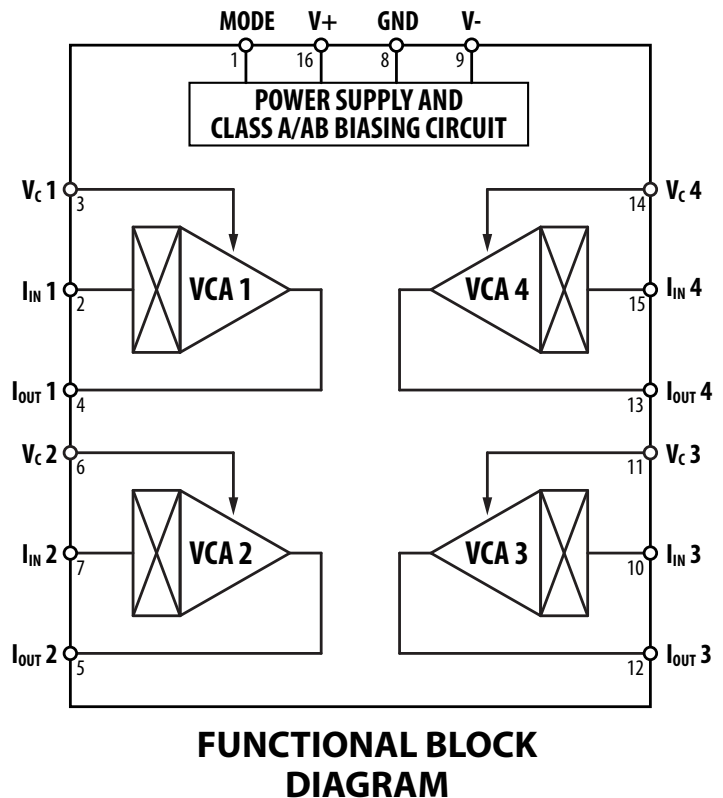
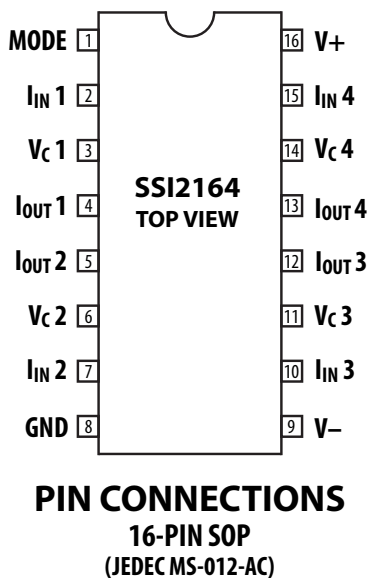
The SSI2164 is a versatile VCA building block for high-performance audio applications. Four independent channels provide voltage control of current-mode inputs and outputs for a gain range from +20dB to -100dB, with control provided by a ground-referenced -33mV/dB constant. The SSI2164 will directly retrofit existing SSM/V2164 positions while offering improvements that include significantly lower overall distortion, on-chip protection against asymmetrical power failure, and a substantial increase of input current handling.

The device offers considerable flexibility for a wide range of design goals and applications. A unique mode control allows selection of Class A, Class AB, or in-between using a single resistor. In addition, improved current handling allows use of considerably lower value input resistors for reduced output noise without loss of headroom. Two or more channels can be parallel-connected for further noise improvement. Finally, SSI2164 VCA channels can be used as high-quality OTA building blocks for a variety of applications such as voltage controlled filters, exponential generators, and antilog converters.

The SSI2164 will operate on supplies as low as +8V for battery-powered devices such as guitar pedals, or up to ±18V in systems where maximum headroom is desired.

### FEATURES

- Improved Direct Replacement for SSM2164/V2164
- Input Current Handling Increased 2x to 1mA
- Pin-Selectable Class A or AB Operation
- 118dB Dynamic Range (Class AB)
- Low Distortion – Typical 0.025% (Class A)
- Large Gain Range: -100dB to +20dB
- ±4V to ±18V Operation
- No External Trimming
- Low Control Feedthrough – Typical -60dB



**SPECIFICATIONS** ( $V_S = \pm 15V$ ,  $V_{IN} = 0.775V_{RMS}$ ,  $f = 1kHz$ ,  $A_V = 0dB$ , Class AB,  $T_A = 25^\circ C$ ; using Figure 1 circuit without diode)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
Supply Voltage Range	$V_S$		$\pm 4$		$\pm 18$	V
Supply Current	$I_S$	Class AB, $V_C = GND$		$\pm 6$	$\pm 8$	mA
Supply Current	$I_S$	Class A, $V_C = GND$ , $I_M = 1mA$		$\pm 8.4$		mA
Power Supply Rejection Ratio	PSRR	60Hz		90		dB
<b>CONTROL PORTS</b>						
Input Impedance			9	10	11	k $\Omega$
Gain Constant		After 60 seconds of operation		-33		mV/dB
Gain Constant Temp. Coefficient				-3300		ppm/ $^\circ C$
Control Feedthrough		$A_V = 0dB$ to $-40dB$		-60		dB
Gain Accuracy		$A_V = 0dB$		$\pm 0.30$		dB
		$A_V = +20dB$		$\pm 0.55$		dB
		$A_V = -20dB$		$\pm 0.55$		dB
Channel-to-Channel Gain Matching		$A_V = 0dB$		0.07		dB
		$A_V = -40dB$		0.24		dB
Maximum Attenuation				-100		dB
Maximum Gain				+20		dB
<b>SIGNAL INPUTS</b>						
Input Bias Current	$I_B$			$\pm 10$		nA
Input Current Handling				1		mA <sub>P</sub>
<b>SIGNAL OUTPUTS</b>						
Output Offset Current		$V_{IN} = GND$		$\pm 150$		nA
Output Compliance				$\pm 100$		mV
<b>PERFORMANCE</b>						
Output Noise		Class AB (20Hz -20kHz, unweighted)				
		$R_{IN/OUT} = 30k\Omega$		-93		dBu
		$R_{IN/OUT} = 20k\Omega$		-96		dBu
		$R_{IN/OUT} = 15k\Omega$		-98		dBu
		$R_{IN/OUT} = 7.5k\Omega$		-101		dBu
		Class A (20Hz -20kHz, unweighted) <sup>1</sup>				
		$R_{IN/OUT} = 30k\Omega$		-81		dBu
		$R_{IN/OUT} = 20k\Omega$		-84		dBu
		$R_{IN/OUT} = 15k\Omega$		-87		dBu
		$R_{IN/OUT} = 7.5k\Omega$		-92.5		dBu
Headroom	HR	1% THD		+22		dBu
Total Harmonic Distortion	THD	Class AB (80kHz BW)				
		$A_V = 0dB$		0.05		%
		$A_V = 0dB$ , $V_{IN} = -17dBu$		0.025		%
		$A_V = +20dB$		0.20		%
		$A_V = -20dB$		0.045		%
		Class A (80kHz BW) <sup>1</sup>				
		$A_V = 0dB$		0.025		%
		$A_V = 0dB$ , $V_{IN} = -5dBu$		0.015		%
		$A_V = +20dB$		0.17		%
		$A_V = -20dB$		0.025		%
Channel Separation		$C_F = 10pF$		-110		dB
Unity Gain Bandwidth	SR	$C_F = 10pF$		500		kHz
Slew Rate				700		$\mu A/\mu s$

<sup>1</sup> $I_M = 1mA$

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	$\pm 20V$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Lead Temperature Range (Soldering, 10 sec)	$260^\circ C$
Mode Current ( $I_M$ ; Pin 1 to Pin 16 via $R_M$ )	2.0mA

**ORDERING INFORMATION**

Part Number	Package Type	Quantity
SSI2164S-TU	16-Lead SOP* - Tube	50
SSI2164S-RT	16-Lead SOP* - Tape and Reel	4000

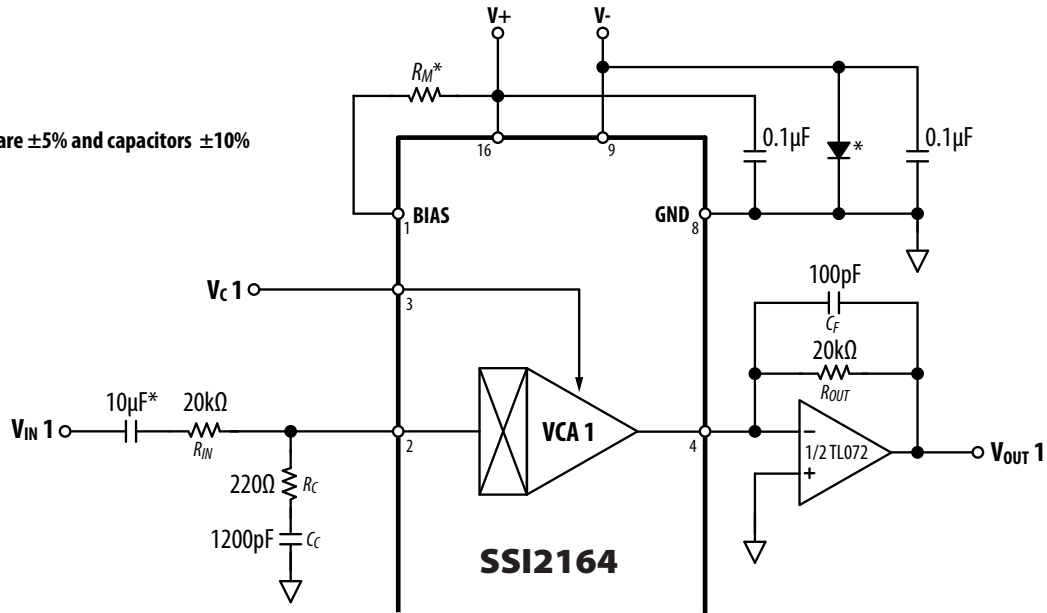
\*Compliant to JEDEC MS-012-AC - Package outline drawing available at [www.soundsemiconductor.com](http://www.soundsemiconductor.com). Please order in full container multiples.

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**NOTES:**

All resistors are ±5% and capacitors ±10%

\*See text



**Figure 1: Typical Application Circuit**

**USING THE SSI2164**

The SSI2164 is a four-channel voltage controlled amplifier with a control range from +20dB to –100dB. Each VCA is an independent current-in, current-out device with a separate voltage control port. Only the mode control affects all four channels; otherwise designers have great latitude on use of each channel for a given application. Basic operation is described below; see the “Principles of Operation” section for further details on inner workings of the device and an application section that follows.

**Inputs**

Figure 1 shows the basic application circuit for one channel. A resistor converts the input voltage to an input current, and a 220Ω resistor in series with a 1200pF capacitor connected to ground ensures stable operation. The SSI2164 is quite tolerant of RC network selection, but 220Ω/1200pF has been proven to work well over a wide range of R<sub>IN</sub> values; existing SSM/V2164 positions with RC networks of 500Ω/560pF also work well for R<sub>IN</sub> of 20kΩ or greater. If desired, compensation can be calculated as follows:

$$R_C = 0.025 \times R_{IN} \quad C_C = \frac{10^{-5}}{R_{IN}}$$

A 20kΩ value for R<sub>IN</sub> is recommended for most applications, but can range from 7.5kΩ to 100kΩ – lower values will produce the best noise performance at some cost in distortion.

Maximum input current handling is approximately 1mA peak. This input current “headroom” is only likely to be a consideration when using R<sub>IN</sub> values of 10kΩ and below with supplies of ±12V and higher. In such cases, one may want to design the signal chain for a maximum input current of 900µA to allow adequate headroom.

An optional series-connected 10µF capacitor is recommended for improved control feedthrough.

**Signal Outputs**

The output current pin should be maintained at virtual ground using an external amplifier such as a TL072; feedback shown results in unity gain. Many op-amps require a feedback capacitor to preserve phase margin. A value of 100pF will suffice in most cases; larger values can be used to reduce high-frequency noise at the expense of bandwidth. In most cases, headroom will be limited by the op amp – increased headroom can be achieved by using a rail-to-rail amplifier or operating on separate supplies.

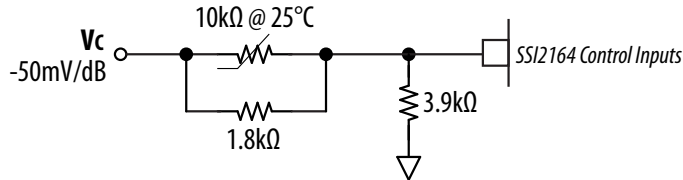
Unlike many VCA’s, output current has the same polarity as the input which simplifies overall design in filter applications. See “Voltage Controlled Filters” in the Application section.

**Control Port**

The SSI2164 provides exponential control with gain constant of -33mV/dB; to realize the full gain range of +20dB to -100dB, control voltage should span from -660mV to 3.3V, respectively. If only attenuation is desired, the control port can be driven directly from a low impedance voltage-output DAC.

The control input has a nominal impedance of 10kΩ. Because of this, any resistance in series with V<sub>C</sub> will attenuate the control signal somewhat. If precise control of gain and attenuation is required, buffering the control voltage is suggested.

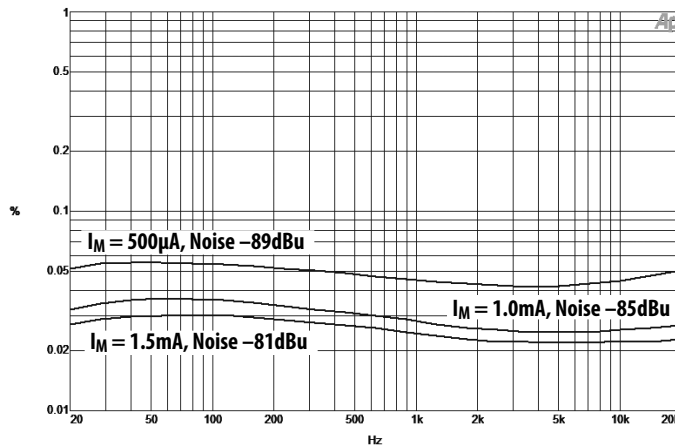
The 33mV/dB control voltage law is essentially set by transistor physics, and has the property of being proportional to absolute temperature, or approximately 0.33%/°C. This is low enough to be unimportant in most applications, but can be reduced with external temperature-dependent networks. One example is shown in Figure 2 using an inexpensive NTC thermistor (such as Vishay NTCLE100E3103JB0 or similar).



**Figure 2: Temperature-Compensated Control Port**

**Class A Mode Current**

The SSI2164’s gain core can be biased as Class A, AB, or in-between. Class AB will yield the best noise performance which is achieved with Pin 1 left open. Class A offers lowest distortion and requires connection of resistor R<sub>M</sub> between Pin 1 and V<sub>+</sub>.



**Figure 3: SSI2164 Class A THD+N At Varying Mode Currents**  
*R<sub>IN</sub> = 20kΩ, V<sub>IN</sub> = 0dBu, A<sub>V</sub> = 0, V<sub>S</sub> = ±15V, 22Hz - 80kHz Filter*

As Figure 3 shows, mode current I<sub>M</sub> affects both noise and distortion. For most applications, a 1mA mode current provides the best overall Class A performance. One can reduce THD further by increasing mode current, but at a significant cost in noise. In addition, increased mode current increases supply current. For example, supply current is typically ±8.4mA with a 1.0mA mode current, but jumps to nearly ±11mA at 1.5mA. Under no circumstances should mode current exceed 2mA. For some applications, the designer might consider mode current below 1mA for improved Class A noise and power dissipation.

Resistor R<sub>M</sub> can be calculated by:

$$R_M = \frac{+V - 0.65V}{I_M}$$

See the “Principles of Operation” section for further discussion on gain core biasing.

**Unused Channels**

If any channels of the SSI2164 are unused, inputs and outputs should grounded. Control pins can be left open or grounded. Rather than put a channel to waste, however, the designer might consider ways to put it to use for additional functionality, or parallel with another channel for reduced noise as described in “Ultra-Low Noise VCA” later in this data sheet.

## Supplies

Supplies from  $\pm 4V$  to  $\pm 18V$  are possible, which should be regulated and include normal design practices such as bypass capacitors as shown in Figure 1. Since internal protections were added to prevent catastrophic failure that may be experienced during SSM/V2164 asymmetrical power-up, the typical Schottky diode solution is no longer necessary. In most applications, no diode is needed. Modular synthesizer sub-systems may want to include a standard 1N4148-style diode as an extra measure of protection since “hot” plugging of modules may be experienced.

Single supply operation is described in the Applications section.

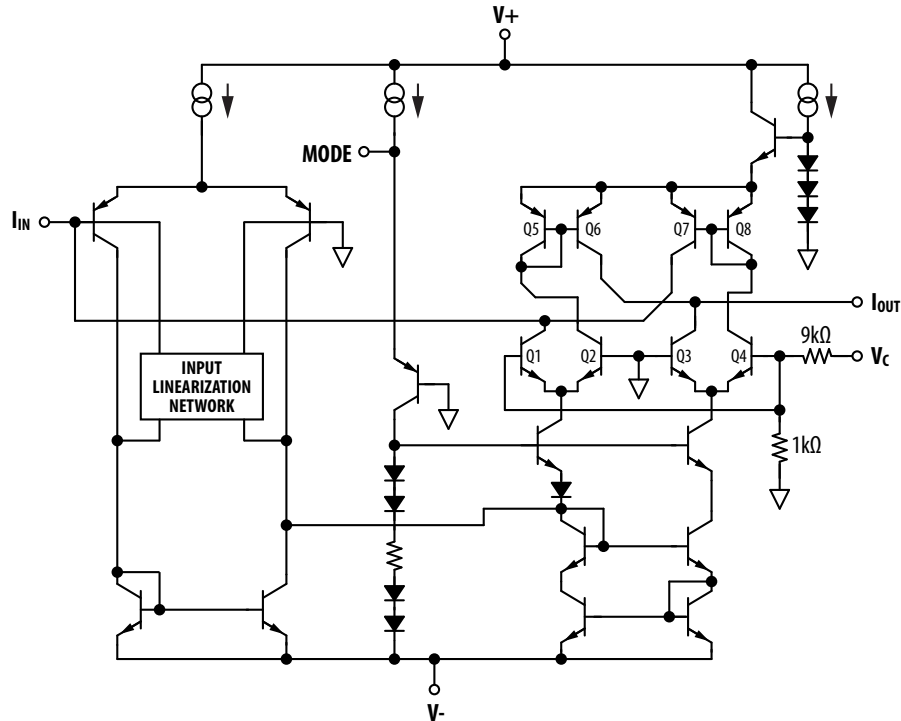


Figure 4: SSI2164 Simplified Schematic

## PRINCIPLES OF OPERATION

### VCA Core

The simplified schematic in Figure 4 shows the basic structure of a VCA cell. The gain core is comprised of matched differential pairs Q1 – Q4 and current mirrors Q5, Q6 and Q7, Q8. The current input pin,  $I_{IN}$ , is connected to the collectors of Q1 and Q7 and the difference in current between these two transistors is equivalent to  $I_{IN}$ . For example, if  $100 \mu A$  is flowing into the input, Q1’s collector current will be  $100 \mu A$  higher than Q7’s collector current.

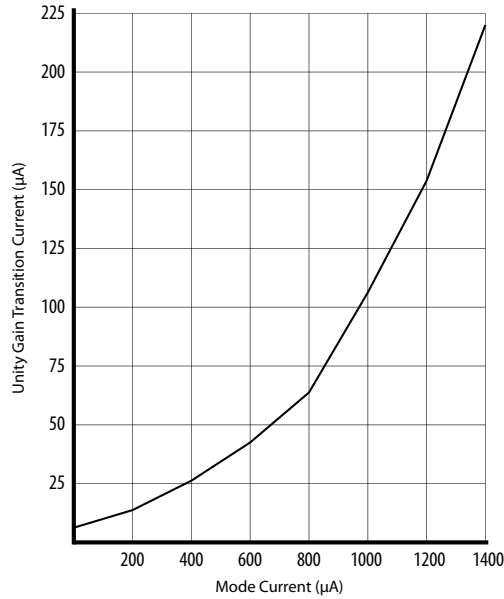
The control voltage  $V_C$  steers the signal current from one side of each differential pair to the other, resulting in either gain or attenuation. For example, a positive voltage on  $V_C$  steers more current through Q1 and Q4 and decreases the current in Q2 and Q3. The current output pin,  $I_{OUT}$ , is connected to the collector of Q3 and the current mirror (Q6) from Q2. With less current flowing through these two transistors, less current is available at the output. Thus, a positive  $V_C$  attenuates the input and a negative  $V_C$  amplifies the input. The VCA has unity gain for a control voltage of 0.0 V where the signal current is divided equally between the gain core differential pairs.

### Biasing the VCA Core

VCA’s operate by modulating differential currents in a transistor core, a fraction of which is steered to the output in a value set by the control voltage. Such VCA’s are generally classified as Class A, Class B and Class AB; terms borrowed from radio transmitter jargon.

In Class A operation the quiescent current in the transistor core is designed to be greater than the maximum input current, so all the transistors remain active at all signal levels. This type of operation produces the lowest distortion, but the high quiescent current level has a severe impact on noise floor and control feedthrough rejection.

In Class B operation the core transistor current is zero and only half the transistors conduct signal at any point of time. Such operation would yield the lowest possible noise floor and near perfect control rejection, but is unfortunately impractical in practice. This is because the transis-



**Figure 5: Class A Mode Current to Transition Current Association**

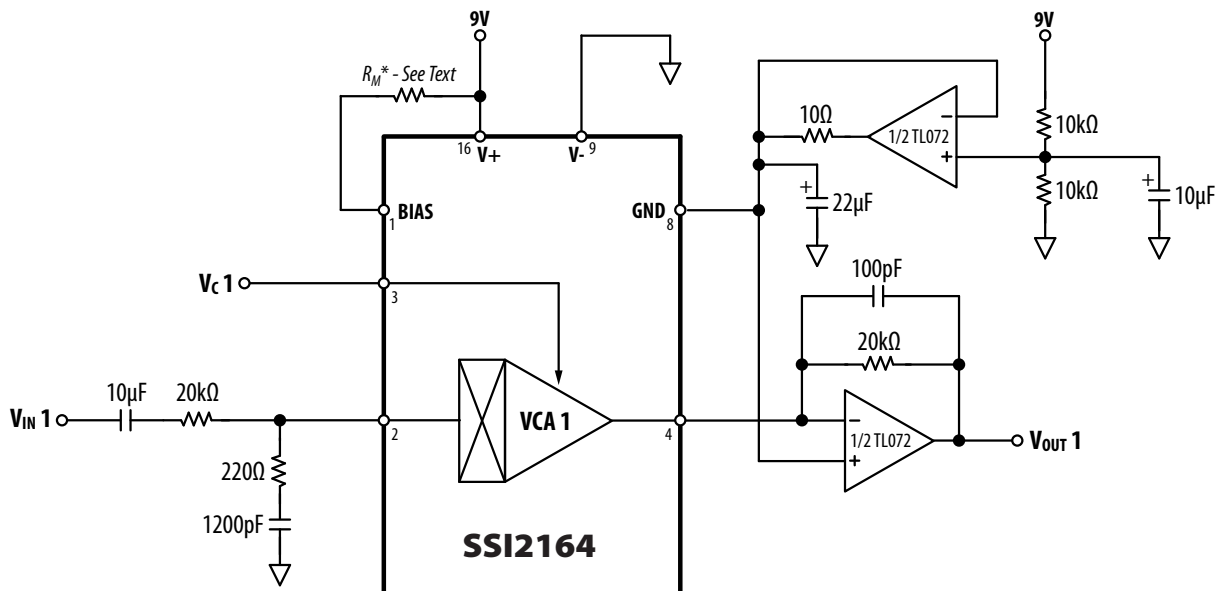
tors effectively disconnect feedback inside the VCA during zero-crossings and low signal levels, potentially causing latch-up or instability. The solution is to arrange the circuit to operate in class A at low signal levels and enter Class B at larger ones. This is known as Class AB operation.

In some applications, distortion may be more important than noise or control feedthrough, in which case it is desirable to raise the point at which the transition from class A to class B takes place. This can be affected by injecting current into the mode pin. The relationship between the input current transition point and the current injected into the mode pin is intentionally non-linear. Figure 5 shows the relationship between the two.

For example, supposing the desired transition point is at a peak input voltage of one volt. With a 20kΩ input resistor this would correspond to an input current of 50µA, and extrapolating from Figure 5 would require a current of about 650µA to be injected into the mode pin. The mode pin is biased about 0.65V above ground, so a resistor placed between this pin and V+ would see a voltage of 14.35V with a +15V supply. Therefore a resistor value of 22kΩ would work well.

## APPLICATION INFORMATION

### SINGLE SUPPLY OPERATION



**Figure 6: Single-Supply Operation**

By referencing to a pseudo-ground point midway between V+ and V-, the SSI2164 can operate from a single supply between +8V and +36V. An op amp provides a low-impedance reference, from which all ground connections are made.

As shown in Figure 6, a voltage divider comprised of two 10kΩ resistors connected to the non-inverting input provides a ground voltage reference, the output of which is connected to ground on the SSI2164. The SSI2164's inputs can be referenced to the same ground, or AC coupled as shown in Figure 6. The 10Ω resistor and 22μF capacitor filter noise that may otherwise be present in the pseudo-ground. Control ports provide unity gain when Vc is equal to the ground reference voltage, or 4.5V in the case of Figure 6.

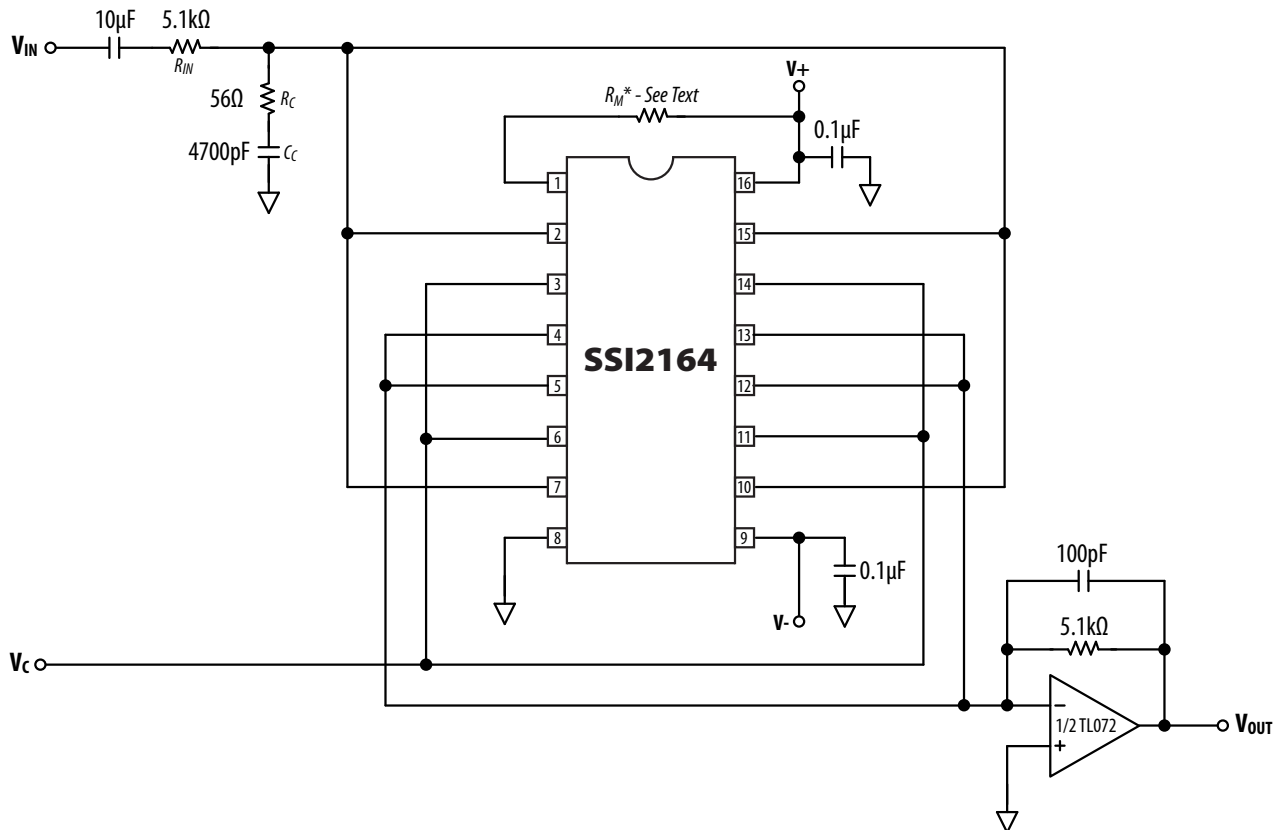
To bias SSI2164 gain cores as class A, the mode resistor value calculation is modified slightly to:

$$R_M = \frac{+V - 0.65V}{2 I_M}$$

For example, if using 9V supplies R<sub>M</sub> should be 3.9kΩ.

### ULTRA-LOW NOISE VCA

Since gain of the SSI2164's input amplifier is finite and well controlled, significant noise improvement can realized by connecting two or more channels in parallel – for example 3dB from two “ganged” channels, 6dB from four channels, and so on. Figure 7 shows a four channel connection. Inputs are tied together, with a single R<sub>IN</sub> and R<sub>C</sub> network placed outside the common connection. Similarly, outputs are connected to a single op amp. Finally, the control ports are tied together for a single V<sub>C</sub>.



**Figure 7: Ultra-Low Noise VCA**

Care must be taken in selecting R<sub>IN/OUT</sub> and R<sub>C</sub> network values. R<sub>IN/OUT</sub> and R<sub>C</sub> are calculated by dividing the desired single-channel value by the number of channels in parallel. Conversely, C<sub>C</sub>'s value is determined by multiplying its single-channel value by the number of channels in parallel. For example, starting with Figure 1 values and four channels paralleled as shown in Figure 7, R<sub>IN/OUT</sub> should be 5.1kΩ, R<sub>C</sub> 56Ω, and C<sub>C</sub> 4700pF. Output noise will improve from -97dBu for a single channel to -103dBu from the four-channel paralleled connection shown.

**FOUR-INTO-ONE-MIXER**

Figure 8 shows a four-channel mixer using the SSI2164. Each input is treated as shown in the Figure 1 typical application, and the four outputs are summed together into a single op amp. A 5.1kΩ R<sub>OUT</sub> value is shown in case some or all inputs expect full-headroom signals. The designer may wish to experiment with R<sub>IN</sub>/O<sub>UT</sub> values to optimize signal handing for a particular application.

Any number of SSI2164 outputs can be tied together for larger mixer input needs.

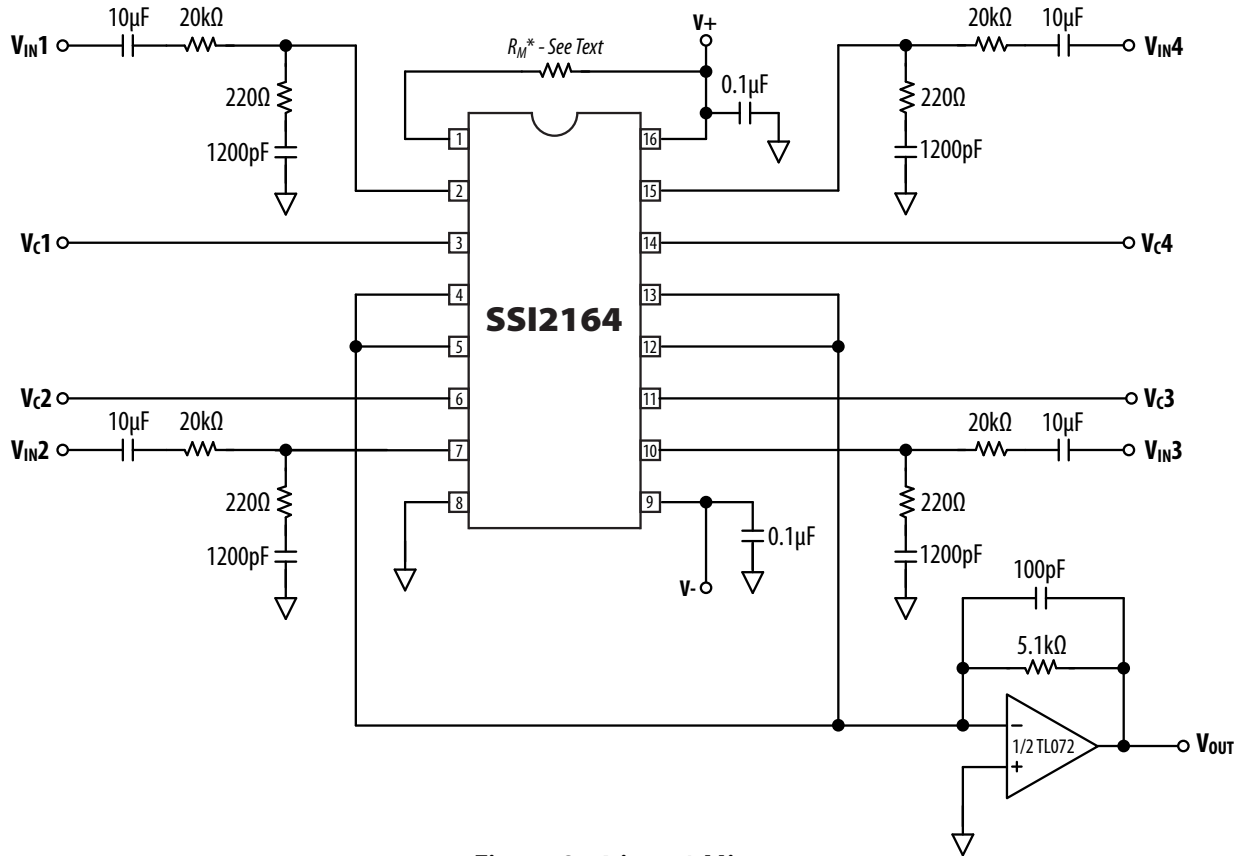


Figure 8: 4-into-1 Mixer

**ZERO TO 5V LINEAR AND EXPONENTIAL CONTROL OPTIMIZED FOR MODULAR SYNTHESIZERS**

By Phillip Gallo

The SSI2164's characteristic -33mV/dB gain constant provides exponential control typical of traditional professional audio VCAs, but some electronic music systems favor linear control. In addition, modular systems often use a control range of 0V to 5V – where 5V corresponds to unity gain and 0V full attenuation – and operate from ±12V supplies. The following circuits address these needs.

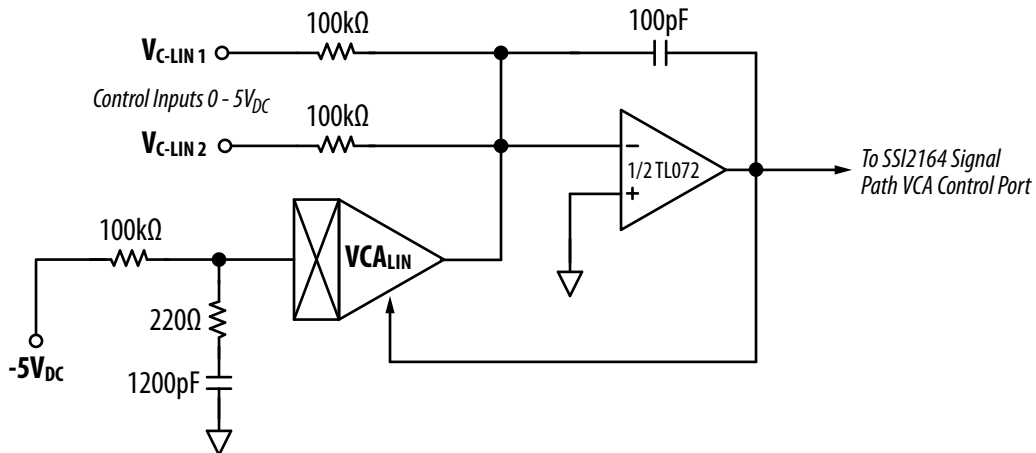


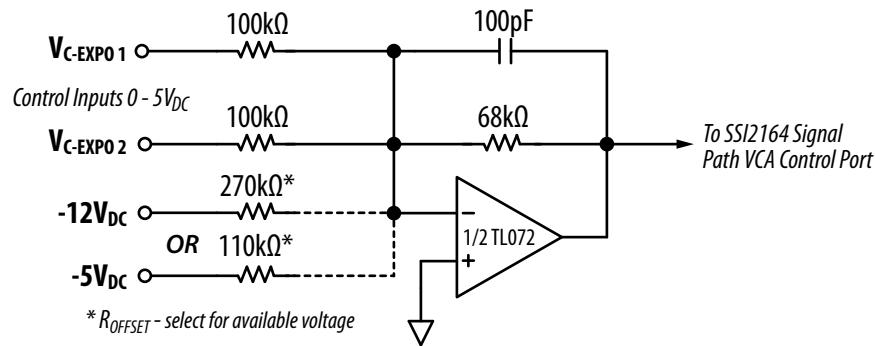
Figure 9: 0 – 5V Linear Control Circuit



Figure 9 depicts a control circuit based on the Irwin linearization scheme (“Op Amp Linearizes Attenuator Control Response,” Mike Irwin, EDN, 7/25/2002, p. 92) which places a SSI2164 VCA channel in the feedback loop of the input control voltage summing amplifier.

The summing amplifier variably adjusts the control VCA to develop negative feedback proportional to applied control inputs. Connecting the circuit output to the control port of a normally configured companion VCA exactly corrects for its exponential control response, resulting in an accurate linear response.

The summing amplifier should be optimally selected for low offset and low input current to exploit the wide dynamic range of a SSI2164 VCA, but a standard TL07x provides adequate performance. The two VCA channels employed should reside within the same component to benefit from thermal and electrical parameter matching.



**Figure 10: 0 – 5V Exponential Control Circuit**

Modular systems also use exponential VCA control over the same positive-going 0V to 5V range. Figure 10 depicts a simple method whereby an op amp sums, inverts, and attenuates the control signal into a negative-going 3.4V signal range compatible with the SSI2164. The feedback resistor value can be adjusted for other signal ranges as needed, such as 34kΩ for the 0-10V control voltages.

Ensuring 0 dB for maximum control voltage is achieved by summing a correction voltage which positively offsets the control output to ensure a 0V output for +5V input. Two different solutions are shown for commonly available voltages.

When a precise gain setting is required, a fixed resistor with a trimmer in series can substitute for R<sub>OFFSET</sub>. Using the 12V example, a 240kΩ resistor with a series 50kΩ trimmer replaces the 270kΩ resistor shown.

Although the examples above show two control inputs, any number of control sources can be summed into the op amps input regardless of configuration type.

**ACCURATE TEMPERATURE COMPENSATED EXPONENTIAL VOLTAGE TO CURRENT CONVERTER**

By Dave Rossum

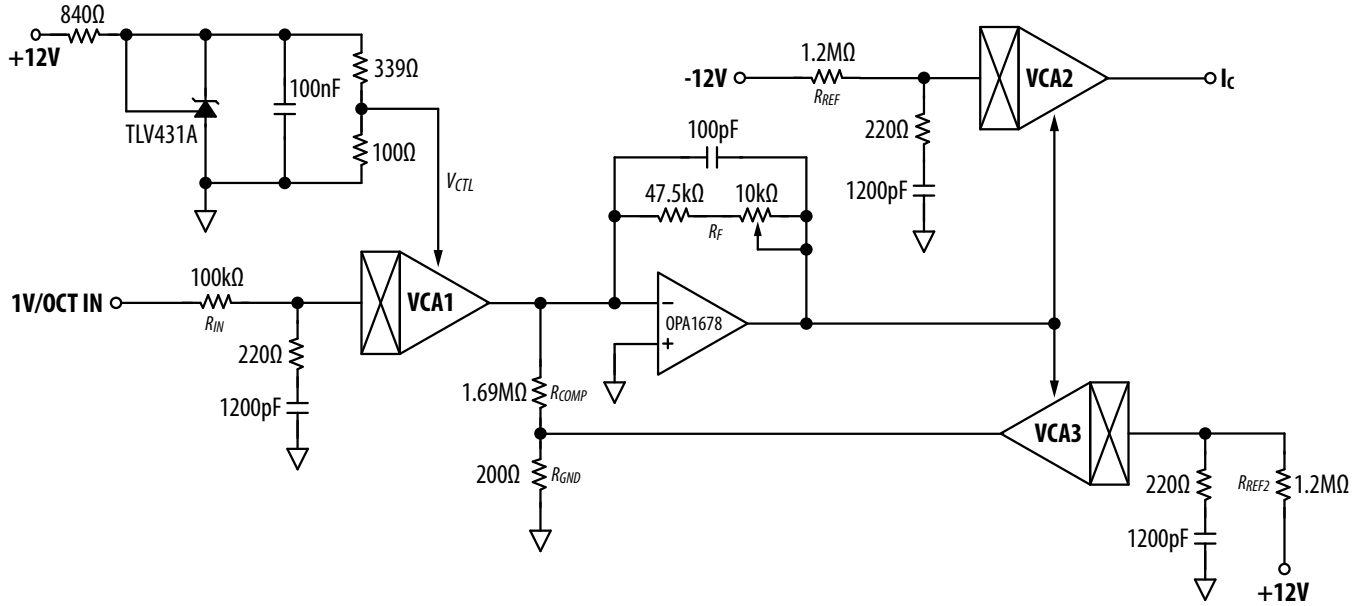
The basic bipolar junction transistor (BJT) exponential generator circuit was first conceived by Alan R. Pearlman of ARP Instruments in 1964. Pearlman knew BJTs accurately obey an exponential relationship between their base-emitter voltage and collector current:

$$I_C = I_S e^{qV_{be}/kT} \tag{1}$$

where I<sub>C</sub> is the exponential collector current output, V<sub>be</sub> is the base-emitter voltage differential, I<sub>S</sub> is a temperature, geometry, and process dependent current specific to the BJT, T is the absolute temperature, q is the electron charge, and k is Boltzmann’s constant. He realized that forcing a known reference collector current I<sub>REF</sub> through one BJT of a matched pair, then adding the resulting voltage to the linear input voltage V<sub>IN</sub> to form the base-emitter voltage of the other BJT of the pair, the variable I<sub>S</sub> term could be eliminated:

$$I_C = I_{REF} e^{qV_{IN}/kT} \tag{2}$$

Pearlman did not deal with the q/kT term. This has been most commonly handled by using a resistor with a known temperature coefficient of 3300ppm/°C as a gain setting element in forming V<sub>IN</sub>. The primary disadvantage of this approach has become the diminishing availability of such “tempco” resistors. An alternative approach, pioneered by Doug Curtis of CEM in 1979, uses a highly linear multiplier circuit whose gain is proportional to the absolute temperature, placed on the same die as the matched BJTs.



**Figure 11: Temperature-Compensated Exponential Voltage to Current Converter**

In 1999, Roman Sowa proposed using the SSM2164 as a temperature compensating multiplier to compensate for the  $q/kT$  factor, in a manner similar to what Curtis devised. The circuit has been used and refined by Osamu Hoshuyama, and Neil Johnson, among others. In this note I present the theory and a practical circuit that has superior accuracy and temperature stability.

The SSI2164 improves upon the SSM2164 by using larger geometry transistors for Q1-Q4 (see Figure 4 in "Principle of Operation"). This makes the revised part more suited than its predecessors for exponential generation.

In Figure 11, the actual exponential generator is created using VCA2.  $I_{REF}$  is supplied by  $R_{REF}$  as a negative current to the VCA2 input, the exponential  $I_C$  is a negative current at the VCA2 output, and the linear control voltage is applied to the VCA2 control port. In this configuration, Q1 and Q2 are essentially off; Q3 is the reference transistor, and Q4 the exponential generator transistor. Note a negative output current is used so as to avoid the lateral PNP transistor current mirror reflecting the output current; a positive current exponential generator thus formed would also work, but is somewhat less accurate.

VCA1 is the  $q/kT$  temperature compensating element. The gain  $G$  of the SSI2164 is:

$$G = I_{OUT} / I_{IN} = e^{-qAV_{CTL}/kT} \quad (3)$$

where  $G$  is the VCA current gain,  $I_{OUT}$  and  $I_{IN}$  are the VCA output and input currents respectively,  $V_{CTL}$  is the SSI2164 control port voltage, and  $A = 0.1$ , the internal 9k:1k ohm attenuation of the SSI2164 control port.

Combining (2) and (3) to represent VCA1 and VCA2 together as in Figure 11:

$$I_C = I_{REF} e^{\left(\frac{qe^{-\frac{qAV_{CTL}}{kT}}}{kT}\right)} \quad (4)$$

The argument of the first exponential should have a zero temperature coefficient:

$$0 = d\left(\frac{qe^{-\frac{qAV_{CTL}}{kT}}}{kT}\right) / dT = \frac{-q(kT - qAV_{CTL})e^{-\frac{qAV_{CTL}}{kT}}}{k^2T^2} \quad (5)$$

Thus when  $V_{CTL} = kT/Aq$ , the circuit is temperature stable. Picking  $T = 325K$ , a temperature in the middle of the expected die temperature range (note 1):

$$V_{CTL} = \frac{1.3807 \times 10^{-23} \times T}{0.1 \times 1.602 \times 10^{-19}} = 0.2801V \quad (6)$$

The final issue is the accuracy of the exponential function itself. While equation (1) applies for an ideal transistor, real transistors have a measurable series emitter resistance  $R_e$ . In the case of the SSI2164,  $R_e$  is modeled at  $0.63\Omega$ . As a result, at (for example) an exponential output current of  $320\mu\text{A}$ , the effective  $V_{be}$  will be low by about  $320\mu\text{A} \times 0.63\Omega = 200\mu\text{V}$ , an error of about 0.75%. This error can be compensated by a second exponential generator (in this case, VCA3 as shown in Figure 9) having the same reference current, a portion of whose output current is routed to the control voltage op amp. Exact compensation is achieved when:

$$R_e = \frac{AR_F R_{GND}}{R_{GND} + R_{COMP}} \quad (7)$$

Note that this compensation circuit can also handle any other errors which are linear with the output current, such as the discharge time of a sawtooth oscillator.

### Design Procedure

1. Choose an operating temperature, and use equation 6 to determine  $V_{CTL}$  (notes 1 and 2).
2. Choose an input impedance  $R_{IN}$  for the 1V/octave input, in this case  $R_{IN} = 100\text{k}\Omega$ . The input to VCA1 is a current summing node, so other control voltage inputs can be summed here.
3. Compute the nominal value of  $R_F = R_{IN} \times V_{CTL} \times e \times \ln(2) = 52.78\text{k}\Omega$  in this case. Typically  $R_F$  will be implemented by a fixed value and a series 1V/oct trimmer whose total nominal value is  $R_F$ .
4. Choose a reference current  $I_{REF}$ , the output current when no current is applied to the input summing node, in this case  $10\mu\text{A}$ .
5. Select a negative reference voltage  $V_{REF}$ , in this case the -12V supply (note 3), and determine the value of  $R_{REF} = R_{REF2} = -V_{REF}/I_{REF} = 1.2\text{M}\Omega$ .
6. Choose an upper limit for optimal accuracy, in this case 5 octaves, and determine the maximum accurate output current  $I_{MAX} = I_{REF} \times 25 = -320\mu\text{A}$ .
7. Choose a convenient value for  $R_{GND}$  such that at  $V = -R_{GND} \times I_{MAX}$  is between 50mV and 100mV, in this case  $R_{GND} = 200\Omega$ .
8. Compute the value of  $R_{COMP} = 0.1 \times R_F \times R_{GND}/R_{COMP} - R_{GND}$ , in this case  $1.69\text{M}\Omega$ . You can adjust  $R_e$  for any other systematic errors linear with output current.
9. The op amp should have low input offset voltage and bias current and temperature coefficients. An OPA1678 is recommended.

SPICE simulations indicate that the circuit of Figure 9 is exponentially accurate to  $\pm 0.12\%$  over 10 octaves at a die temperature of 325K, and maintains its accuracy over 10 octaves and temperatures from 310K to 330K ( $20^\circ\text{C} - 40^\circ\text{C}$  ambient) to within 0.25%.

### Additional Notes

1. SSI2164 current consumption is typically 6mA when in class AB mode (recommended), or 144mW at  $\pm 12\text{V}$  supplies. The SOP16 package typical junction to ambient thermal resistance is  $118^\circ\text{C}/\text{W}$ , predicting a die temperature  $17^\circ\text{C}$  above ambient. Assuming ambient to be nominally  $35^\circ\text{C}$ , the nominal die temperature is  $52^\circ\text{C} = 325\text{K}$ . Since the second order tempco error is larger at higher temperatures than lower, overestimating this nominal temperature is preferred.
2.  $V_{CTL}$  should be accurate to 1% or better; use of a band-gap reference is recommended, and if resistively divided, the source impedance kept low to eliminate any effect of the wide tolerance on the  $10\text{k}\Omega$  control port input impedance of the SSI2164.
3. The negative voltage reference should be temperature stable to  $100\text{ppm}/^\circ\text{C}$ ; while the negative power supply is used as illustration, most designs will use a more stable reference voltage. Also note a linear modulation of the output current can be implemented by adding a modulation current to  $I_{REF}$  at the VCA2 input summing node, and this linear modulation can potentially be "through zero."

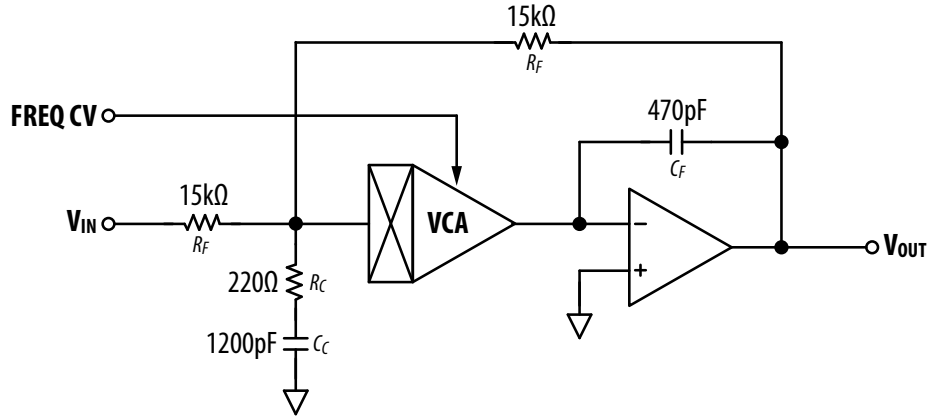
## VOLTAGE CONTROLLED FILTERS

*By Rutger Vlek*

The SSI2164 is a versatile high-performance device that can be used to construct a variety of building blocks for analog or hybrid synthesizers, effect units, and other audio equipment. While voltage controlled amplifiers are its most obvious application, the SSI2164 also excels in voltage controlled filters with low noise, high headroom, built-in exponential control law, and small footprint.

### Building Blocks for Voltage Controlled Filters

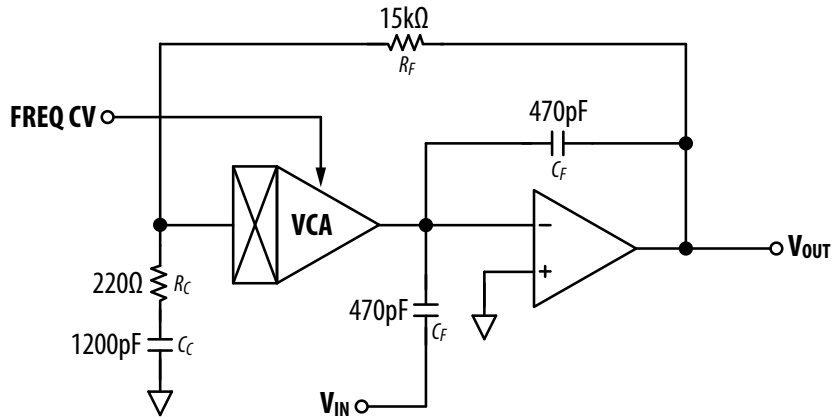
Figure 12 shows the basic circuit for a 6dB/octave (1-pole) low-pass filter. The cutoff frequency can be controlled via the FREQ CV control of a SSI2164. In this circuit, the SSI2164 is analogous to a voltage controlled resistor. Capacitor  $C_f$  forms the core of an inverting integrator, and



**Figure 12: Low-Pass Filter Stage**

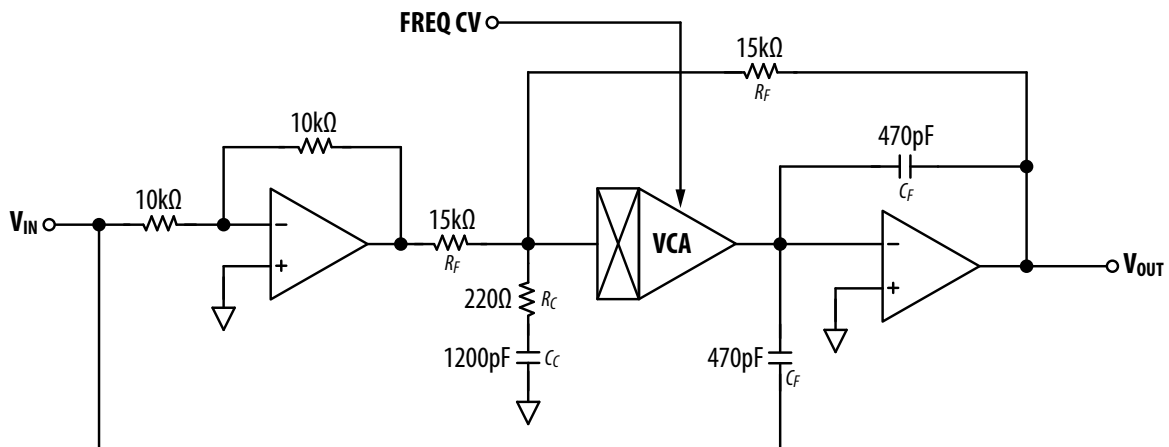
is being charged or discharged by the input (left-most  $R_F$ ) and feedback path (right-most  $R_F$ ) currents at a rate determined by the SSI2164 'resistive' element. Capacitor  $C_C$  and resistor  $R_C$  make up a compensation network for stable operation of the SSI2164 internal circuitry.

In a similar fashion, Figure 13 shows a 6dB/octave high-pass filter. The input signal enters the circuit at the virtual ground summing node of an op amp, after which a low-pass filtered version is subtracted from the raw input, courtesy of the negative feedback loop via  $R_F$ . The resulting response is that of a high-pass filter.  $C_C$  and  $R_C$  make up the compensation network for the SSI2164.



**Figure 13: High-Pass Filter Stage**

Figure 14 shows a voltage controlled all-pass filter, which is commonly used in phase shifter or phaser effects, but also serves various other purposes. It combines aspects from both the low and high-pass filters, supplied with a common input signal. This results in a flat frequency response, but a phase response that changes radically around the so-called corner frequency which is brought under voltage control via the



**Figure 14: All-Pass Filter Stage**

SSI2164. In order to obtain the required phase shift, the signal to the low-pass input (via left-most  $R_F$ ) needs to be inverted, which is done by an inverting opamp in front of the SSI2164.

For all of the above mentioned filter stages, the relation between control voltage ( $Freq_{CV}$ ) and cutoff or corner frequency  $f$  (in Hz) is described by Equation 8, where  $R_F$  and  $C_F$  match with the component labels in the schematics. As the control law of the SSI2164 is exponential, an external exponential convertor is not required.

$$f = \frac{1}{2\pi R_F C_F} 10^{\frac{3}{2} Freq_{CV}} \quad (8)$$

Filters with steeper slopes (e.g. 12 or 24dB/octave) can be constructed by cascading multiple filter stages, while sharing a single control input signal. Band-pass responses can be obtained by combining low and high-pass filter stages. Figure 15 shows a few of the most popular filter designs achieved with cascaded stages. All of them can be turned into a resonant filter by feeding a controlled and inverted amount of output back into the input. Bear in mind that the low-pass filter stage in Figure 12 is already inverting the signal.

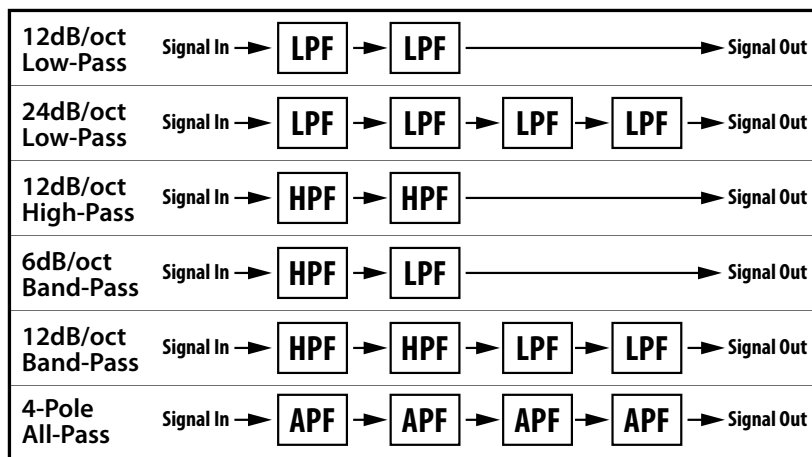


Figure 15: Various Filter Configurations

### Generic CV driver

Practical application of the above mentioned filter stages usually calls for a physical control (potentiometer) and/or control voltage input, signal scaling and some protection. The circuit in Figure 16 takes care of this and can be used for driving one or several filters stages. A potentiometer provides direct control over cutoff or corner frequency. A 1V/octave control signal could be fed into the inverting input through a 100kΩ resistor. The ratio between ( $R_1$ ,  $R_2$ ) and  $R_3$  determines the scaling, and if accurate tuning is required  $R_3$  should be replaced by a trimmer.  $C_1$  filters unwanted noise from the control signal, allowing the SSI2164 to reach best performance. Diodes  $D_3$  and  $D_4$  restrict the control signal to a maximum of approximately 0.5V.

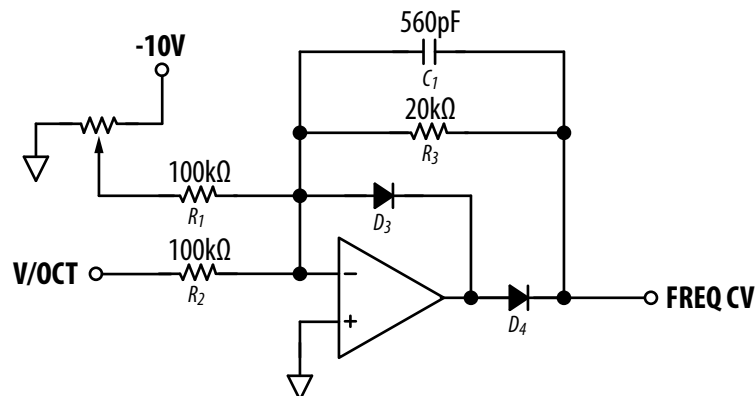


Figure 16: Generic CV Driver

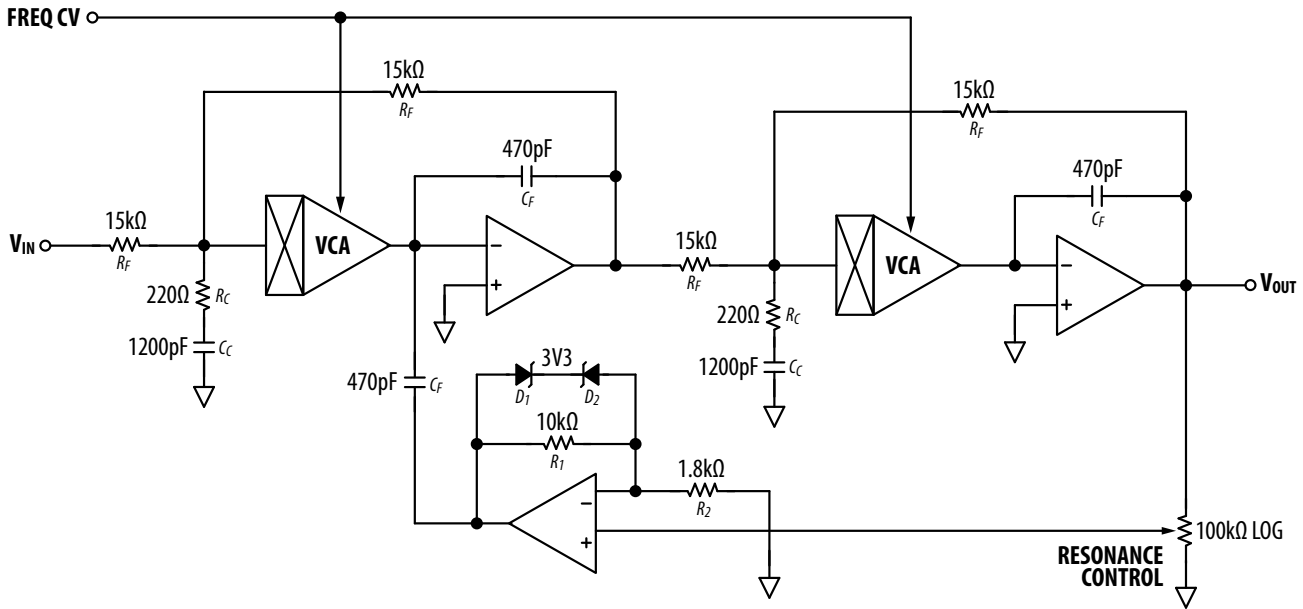
**Component Selection**

The above mentioned filter stages require an opamp with a relatively low input bias current. The ubiquitous TL074 works well; a more modern device such as the OPA1679 provides additional advantages with respect to noise performance, distortion and headroom.

Capacitor(s)  $C_F$  are key to accurate frequency and phase performance. Most suitable are capacitors with a high temperature stability (NPO / COG type) and low-tolerance ( $\leq 2\%$ ). Low tolerance is especially important for the performance of the high-pass and all-pass stages.

**Example: 2-pole Resonant Low-Pass Filter**

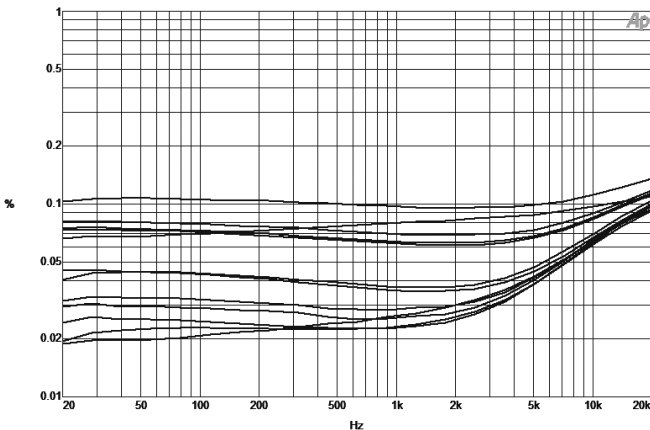
Figure 17 describes a full resonant 12dB/octave (2-pole) low-pass filter as commonly used in analog synthesizers. It is composed of two low-pass filter stages, and adds a negative feedback loop through a potentiometer (for resonance control) and a soft-limiter. The maximum amount of resonance is set by the value of  $R_2$ . Two 3.3V Zener diodes  $D_1$  and  $D_2$  restrict the maximum resonance amplitude, and contribute to a smooth sine-like wave at self-oscillation. Signal input level should be around 5 to 10Vpp. Cutoff frequency control can be obtained by using the CV driver in Figure 16. Pin 1 (mode) of the SSI2164 is left unconnected, in order to operate in class-AB mode for best noise performance. This filter can be easily transformed into a 4-pole variation by cascading two more low-pass stages, feeding the resonance loop from the last stage, and adjusting  $R_2$  for the desired maximum resonance level. Please remember that Zener diodes inherently have some capacitance, which will start to affect the high-frequency resonance response when larger values for  $R_1$  are used.



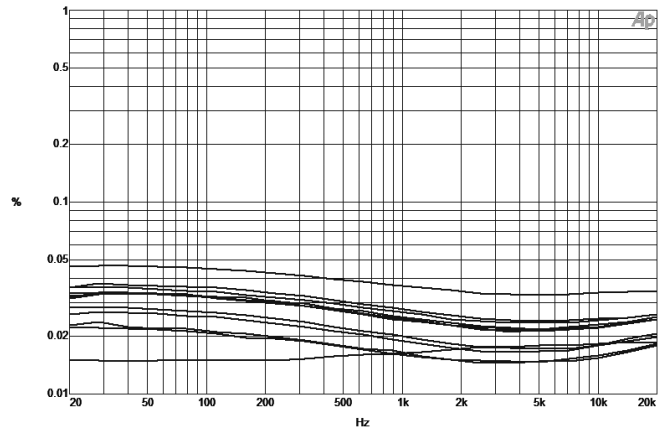
**Figure 17: 2-Pole Resonant Low-Pass Filter**

**TYPICAL PERFORMANCE GRAPHS\***

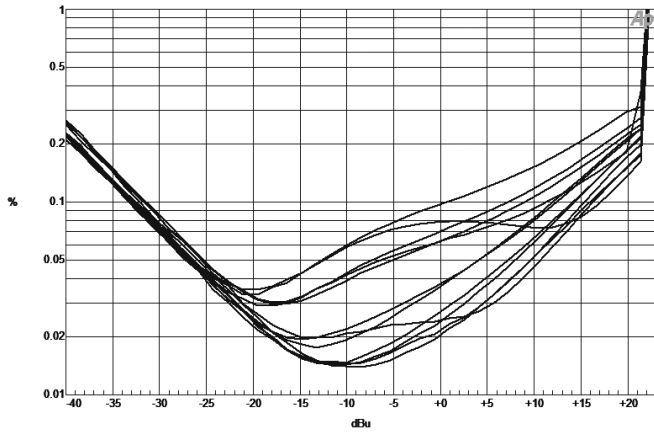
Figure 1 Application Circuit at  $V_S = \pm 15V$ ,  $A_V = 0dB$ ,  $V_{IN} = 0dBu$ ,  $R_{IN/OUT} = 20k\Omega$ ,  $f = 1kHz$ ; unless otherwise noted



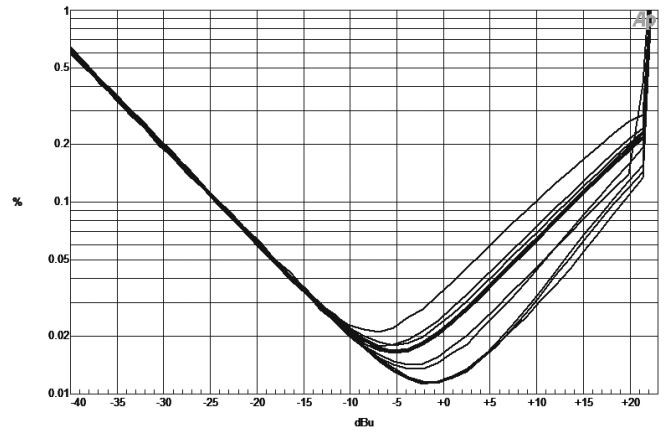
**THD+N vs. Frequency Distribution - 12 Channels**  
Class AB, 22Hz - 80kHz Filter



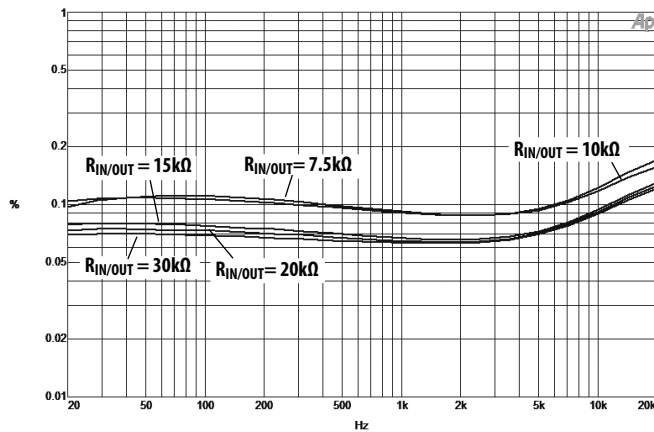
**THD+N vs. Frequency Distribution - 12 Channels**  
Class A, 22Hz - 80kHz Filter



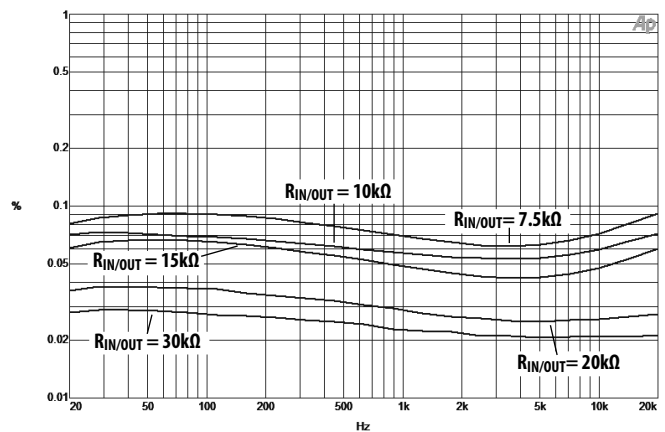
**THD+N vs. Amplitude Distribution - 12 Channels**  
Class AB, <10Hz - 22kHz Filter



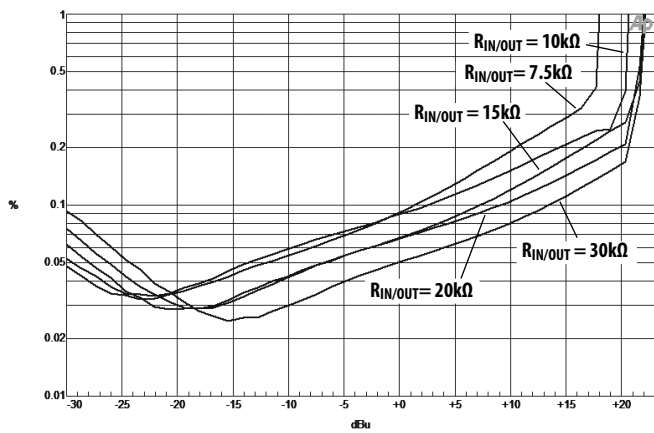
**THD+N vs. Amplitude Distribution - 12 Channels**  
Class A, <10Hz - 22kHz Filter



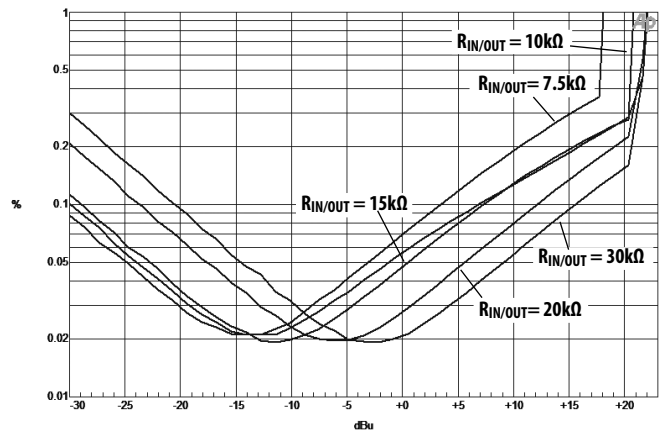
**THD+N vs. Frequency vs.  $R_{IN/OUT}$**   
Class AB, 22Hz - 80kHz Filter



**THD+N vs. Frequency vs.  $R_{IN/OUT}$**   
Class A, 22Hz - 80kHz Filter



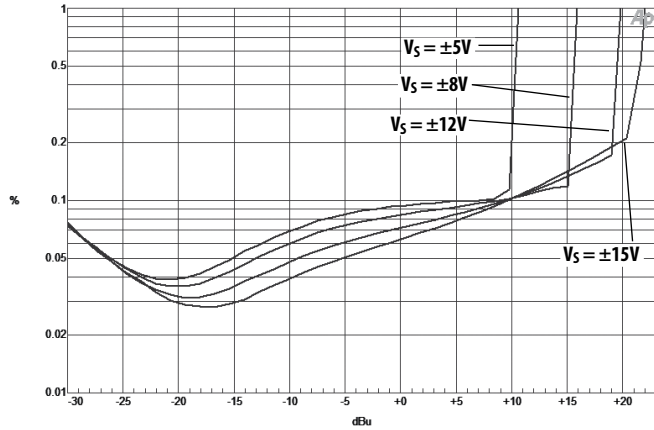
**THD+N vs. Amplitude vs.  $R_{IN/OUT}$**   
Class AB, <10Hz - 22kHz Filter



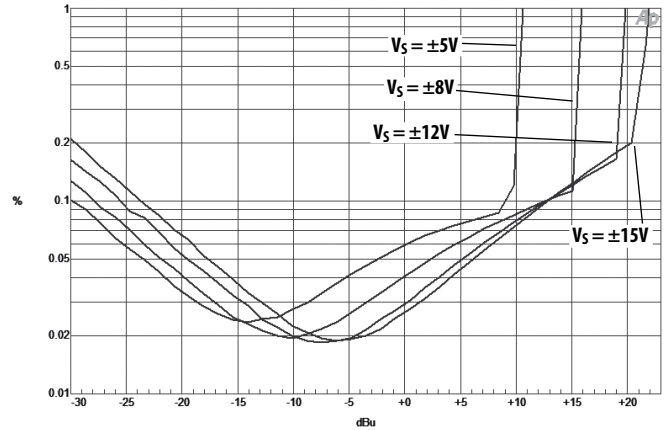
**THD+N vs. Amplitude vs.  $R_{IN/OUT}$**   
Class A, <10Hz - 22kHz Filter

**\*About THD+Noise data.** As the name implies, THD+N measures total harmonic distortion *and* noise. In all cases, THD *without* noise will be lower than shown. The noise component will increasingly dominate graph data as signal levels decrease, for example, in THD+N vs. Amplitude graphs. Similarly, an otherwise “apples to apples” comparison between two lines under different noise conditions such as Class A vs. Class AB or differing  $R_{IN}$  values may be affected. While one might dismiss the value of THD+N noise measurements, recall that both distortion and noise are undesirable so such information therefore shows all the things you *don't* want, which may be very useful when setting design limits.

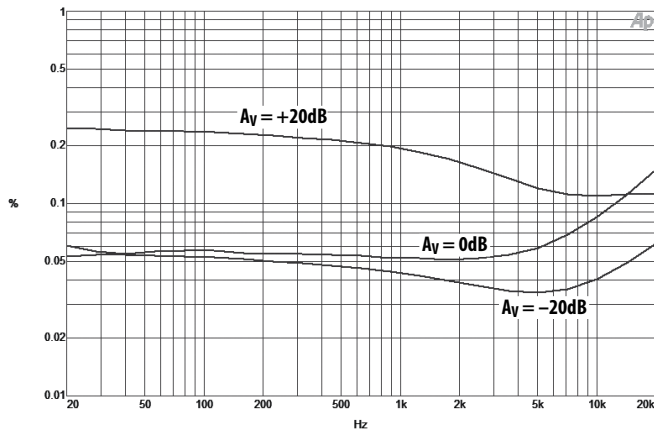




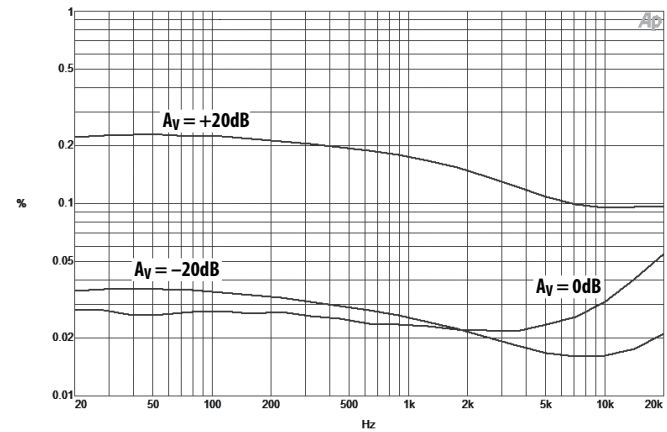
**THD+N vs. Amplitude vs. Supply Voltage**  
*Class AB, <10Hz - 22kHz Filter*



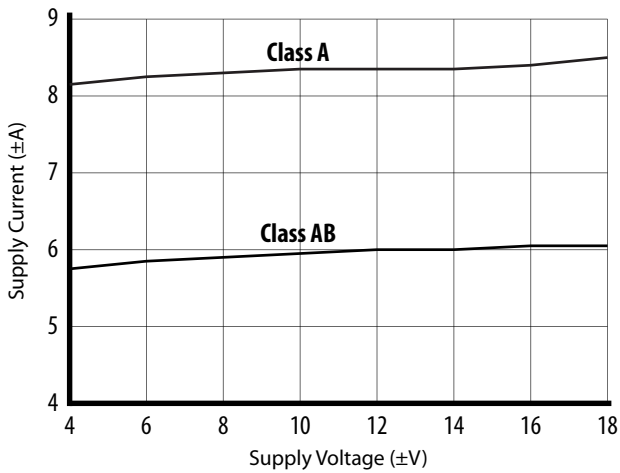
**THD+N vs. Amplitude vs. Supply Voltage**  
*Class A, <10Hz - 22kHz Filter*



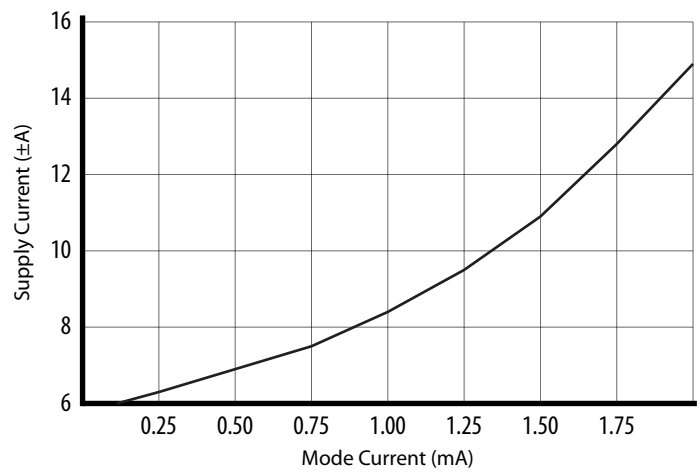
**THD+N vs. Frequency vs. Gain**  
*Class AB, 22Hz - 80kHz Filter*



**THD+N vs. Frequency vs. Gain**  
*Class A, 22Hz - 80kHz Filter*



**Supply Current vs. Supply Voltage**



**Supply Current vs. Mode Current**

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